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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/922,755	08/06/2001	Christopher M. Giles	99-412	9570

7590 06/03/2004

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EXAMINER	
BADERMAN, SCOTT T	

ART UNIT	PAPER NUMBER
2113	7

DATE MAILED: 06/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

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Office Action Summary	Application No.	Applicant(s)	
	09/922,755	GILES, CHRISTOPHER M.	
	Examiner	Art Unit	
	Scott T Baderman	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 August 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-12* is/are allowed.

6)☒ Claim(s) *13,15 and 17* is/are rejected.

7)☒ Claim(s) *14,16 and 18-25* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 August 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 2.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 1 is objected to because of the following informalities: In line 3, the term "improvement" should be deleted. In line 8, the term "other" should be inserted before "processor". Appropriate correction is required.

2. Claim 15 is objected to because of the following informalities: In line 5, the term "the debug event signal" lacks antecedent basis. See claim rejection below for Examiner's interpretation. Appropriate correction is required.

3. Claim 17 is objected to because of the following informalities: In line 3, "debut" should be "debug". In line 4, the term "the debug event signal" lacks antecedent basis. See claim rejection below for Examiner's interpretation. Appropriate correction is required.

Allowable Subject Matter

4. Claims 1-12 are allowed.

5. The following is an examiner's statement of reasons for allowance:

With respect to claim 1, the Examiner asserts that the novelty of the claim, when read as a whole, is "a debug interface associated with each one processor which *asserts a debug event*

signal when the associated one processor enters the debug mode as a result of incurring an internal debug event, a logic circuit associated with each processor and *receptive of the debug event signal supplied by each processor of the system*, wherein each logic circuit *responds to the debug event signal supplied by each other processor to assert an external debug break signal* to the processor associated with the logic circuit, and the *debug interface further responds to the external debug break signal supplied by the associated logic circuit to place the processor into the debug mode*" (emphasis added).

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

6. Claims 14, 16 and 18-25 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 13, 15 and 17 are rejected under 35 U.S.C. 102(b) as being anticipated by Hirayama (6,031,991).

As in claim 13, Hirayama discloses a method for simultaneously halting execution of instructions by each processor of a system having multiple processors upon one of the processors of the system entering a debug mode of operation as a result of incurring a debug event (i.e., when one of the processors detects an error and generates a trap signal, all of the processors enter a debug mode simultaneously, wherein their respective instructions are halted from execution) that comprises halting execution of instructions by the one processor to place that one processor into a debug mode of operation upon that one processor incurring a debug event (i.e., when any of the processors enter a debug mode upon incurring a debug event (detecting an error and generating a trap signal), their respective instructions are halted from execution), and placing each other processor of the system into a debug mode of operation simultaneously with the one processor entering the debug mode of operation by sending an external debug break signal (via the detecting and restart-executing sections) to each other processor of the system to cause each other processor to enter the debug mode of operation (i.e., the detecting and restart-executing sections, upon receiving the trap signal from the one processor, shift the other processors into a debug mode simultaneously with the one processor (Figure 2, column 1: lines 29-37, column 2: line 64 – column 3: line 44, column 4: lines 29-46).

As in claim 15, Hirayama discloses placing each other processor into the debug mode by the assertion of the external debug break signal to each other processor (via the detecting and restart-executing sections), and asserting the external debug break signal to each other processor in response to the one processor asserting a debug event signal (i.e., detecting an error and generating a trap signal) (Figure 2, column 1: lines 29-37, column 2: line 64 – column 3: line 44, column 4: lines 29-46).

As in claim 17, Hirayama discloses utilizing a logic circuit associated with each processor to generate an external debug break signal (via the detecting and restart-executing sections) for the associated processor, and applying a debug event signal (detecting an error and generating a trap signal) from the one processor to the logic circuit associated with each other processor (i.e., when any one processor detects an error and generates a trap signal, that processor is responsible for putting the other processors into the debug mode via the detecting and restart-executing sections) (Figure 2, column 1: lines 29-37, column 2: line 64 – column 3: line 44, column 4: lines 29-46).

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

See Form PTO-892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott T Baderman whose telephone number is (703) 305-4644. The examiner can normally be reached on Monday-Friday, 6:45 AM-4:15 PM, first Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (703) 305-9713. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Scott T Baderman
Primary Examiner
Art Unit 2113

STB